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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,998	01/20/2004	Fang-Bin Liu	250210-1040	1645

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/760,998	LIU, FANG-BIN	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/22/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 3/22/06 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

Figure 1A_B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification appears to be a literal translation into English from a foreign document and is replete with grammatical and idiomatic errors.

The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:

(Page 1)

"The present invention relates to a test of bus connections between components, and in particular to a method and circuit for performing an on-board test of connections between field programmable gate arrays (FPGAs). of the bus can be tested functionally by the method"

"Currently, pin functionality is tested by X-ray and an pattern estimation program or operator successively. "

The examiner would like to point out that throughout the present specification and claims, there are references to "onboard" and "pins". The specification (as understood by the examiner) seems to be describing a method of testing FPGA connections within an integrated circuit. The term "onboard" would imply a board test while "on chip" would imply on an integrated circuit. However, Applicant also uses the term "pins" frequently enough that it is unclear whether this test is to be performed on connections of chips on a circuit board or within an integrated circuit. The drawings

would imply an IC as would the background. Clarification is required for proper examination of this application.

Page 2

"The method comprises the steps of disposing a first connection circuit on a first programmable array circuit, such as FPGA, according to a preset LFSR polynomial, disposing a second connection circuit on a second programmable array circuit, wherein pins of the second connection circuit are connected to the corresponding pins of the first connection circuit in one-pin-to-one-pin and parallel layout. In one example, one of the two connection circuits has an XOR gate and the other circuit has a shift register. In another example, one circuit has both an XOR gate and a shift register. A pattern is input to the shift register to be processed by the shift register and a specific pattern is produced from an output pin of the shift register is corresponding to the connection status and relevant information about the first and the second connection circuits. The shift register comprises a plurality of D-type flip-flops connected in serial"

First, it is unclear how a pattern is input to the shift register.

Second, it is unclear how a shift register of D-type flip-flops would 'process' a pattern. This type shift register would merely shift the pattern out.

Third, not only is it unclear how an output pin would 'produce a specific pattern', but it is also unclear how or why a shift register would have an output pin.

The remainder of the sentence is also unclear.

These types of inconsistent statements are replete throughout the entire specification. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claim 1, lines 14-18, it is not disclosed how a pattern is input to the shift register. It is unclear how a shift register of D-type flip-flops would 'process' a pattern. This type shift register would merely shift the pattern out. Not only is it undisclosed how an output pin would 'produce a specific pattern', but it is also unclear how or why a shift register would have an output pin.

As per claim 8, lines 14-17 it is not disclosed how a pattern is input to the shift register. It is unclear how a shift register of D-type flip-flops would 'process' a pattern. This type shift register would merely shift the pattern out. Not only is it undisclosed how

an output pin would 'produce a specific pattern', but it is also unclear how or why a shift register would have an output pin.

Claims 2-7 and 9-13 are dependent on the independent claims 1 and 8, and therefore inherit the 35 U.S.C. 112, first paragraph issues of the independent claims and will not be further considered with respect to their individual merits.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1 and 8, throughout the present specification and claims, there are references to "onboard" and "pins". The specification (as understood by the examiner) seems to be describing a method of testing FPGA connections within an integrated circuit. The term "onboard" would imply a board test while "on chip" would imply on an integrated circuit. However, Applicant also uses the term "pins" frequently enough that it is unclear whether this test is to be performed on connections of chips on a circuit board or within an integrated circuit. The drawings would imply an IC as would the background.

It also seems that applicant is possibly using the term "shift register" interchangeably with LFSR. This could cause further misinterpretations of the claimed invention.

Clarification is required for proper examination of this application.

Claims 2-7 and 9-13 are dependent on the independent claims 1 and 8, and therefore inherit the 35 U.S.C. 112, second paragraph issues of the independent claims and will not be further considered with respect to their individual merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 8 (as understood by the examiner) are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. U.S. Pre Grant publication 2002/0078412.

As per claims 1 and 8 Wang et al. teach the claimed method of testing a programmable logic device having defined programmable function blocks with

programmable interconnects, comprising the steps of (a) configuring, by programming, two or more similar groups of the function blocks and interconnects into identical state machines; (b) operating the programmed state machines by clock and reset signals to generate individual original signatures on global interconnect lines; and (c) comparing the original signatures of the two or more state machines for fault detection. The method further comprises a step for receiving original signatures from different programmed groups of function blocks and interconnects at different dedicated test output blocks, comparing the signatures at the test output blocks, and passing the results of compare to further serially-connected test output blocks connected to further programmed function blocks and interconnects for further comparison. There is a further step for receiving sequential data at a signature analyzer, reducing the data received to a single word by means of a linear feedback shift register circuit, and comparing the final word with a stored expected word to indicate pass or fail for the tested circuit. Paragraphs [0009-0011]

Tests are done selectively for circuitry regions on a candidate IC. For example, for some ICs the logic and interconnect elements may be consistent row by row and column by column, and for some ICs the elements may be less consistent, such that portions of rows and columns may have to be configured differently to make state machines that will test all of the logic and interconnect functionality. The structure of a candidate PLD will determine the configuration and the order in which testing may be done. One may therefore configure and conduct a series of tests that will fully test a

portion of the overall candidate device, and then configure and test another portion, until the entire device is thoroughly tested. Paragraph [0037]

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138